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**Yu et al.**

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(54) **PACKAGE WITH MULTIPLE PLANE I/O STRUCTURE**

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*H01L 2224/16227*; *H01L 2924/15311*; *H01L 24/17*; *H01L 24/13*  
USPC ..... 257/278, 713, E21.614, 712; 438/24, 26  
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*H01L 21/56* (2006.01)  
*H01L 23/31* (2006.01)  
*H01L 25/065* (2006.01)

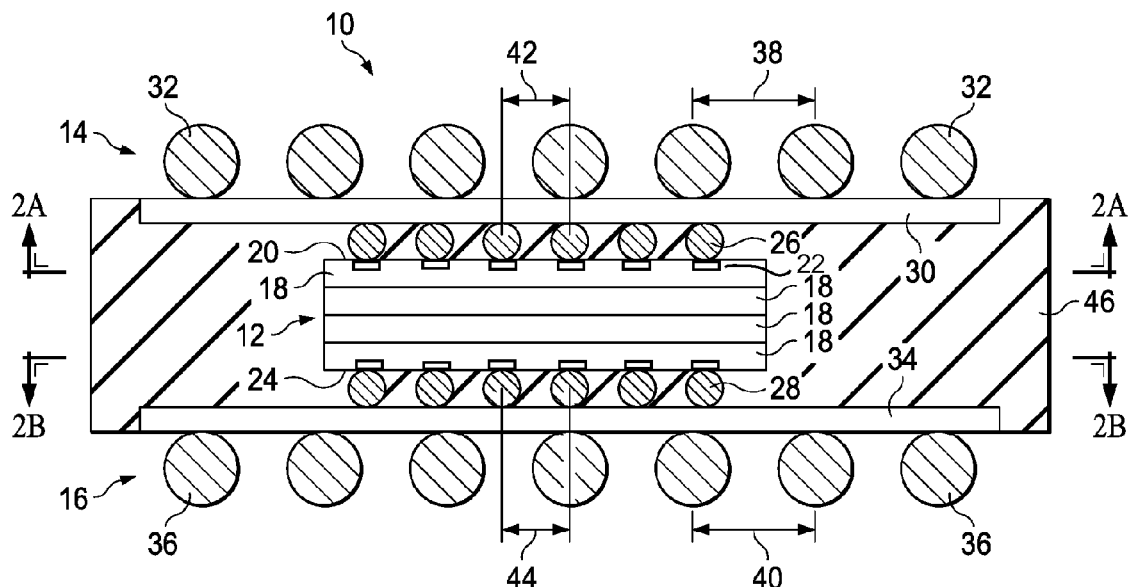
(52) **U.S. Cl.**

CPC ..... *H01L 24/17* (2013.01); *H01L 21/56* (2013.01); *H01L 23/3107* (2013.01); *H01L 23/49816* (2013.01); *H01L 23/49833* (2013.01); *H01L 23/49838* (2013.01); *H01L 24/81* (2013.01); *H01L 25/065* (2013.01); *H01L 2224/16225* (2013.01); *H01L 2224/16227*

(57) **ABSTRACT**

A embodiment package includes a three dimensional integrated circuit (3D IC) with first input/output pads on a first side and second input/output pads on a second side, a first fan out structure electrically coupled to the first input/output pads on the first side of the three dimensional integrated circuit, and a second fan out structure electrically coupled to the second input/output pads on the second side of the three dimensional integrated circuit.

**20 Claims, 4 Drawing Sheets**



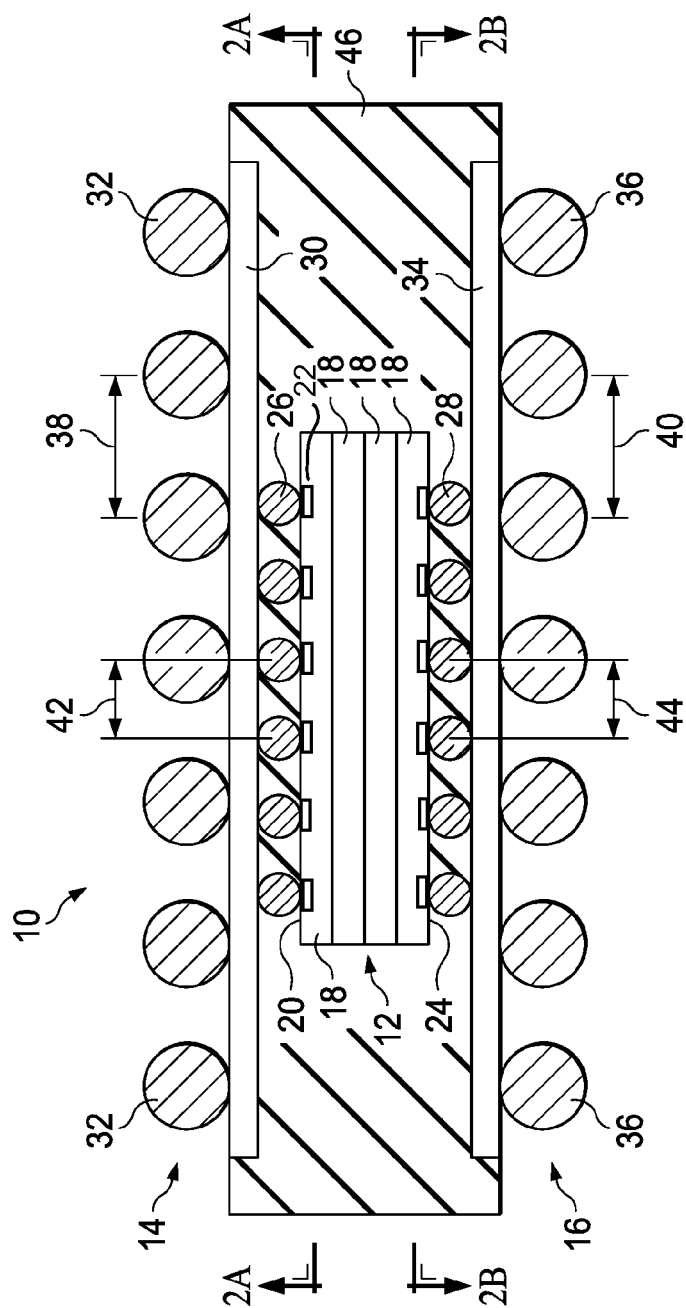


FIG. 1

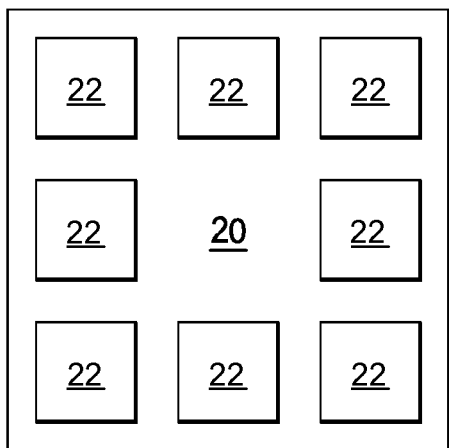


FIG. 2A

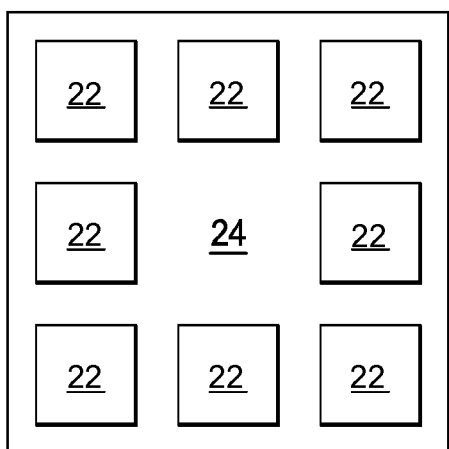


FIG. 2B

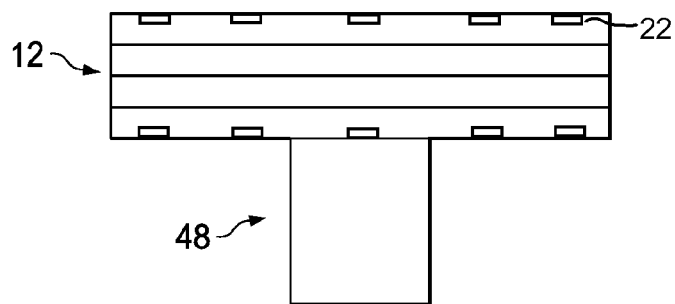


FIG. 3A

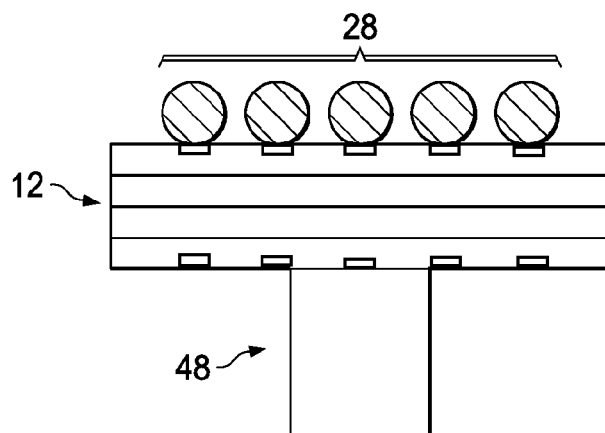


FIG. 3B

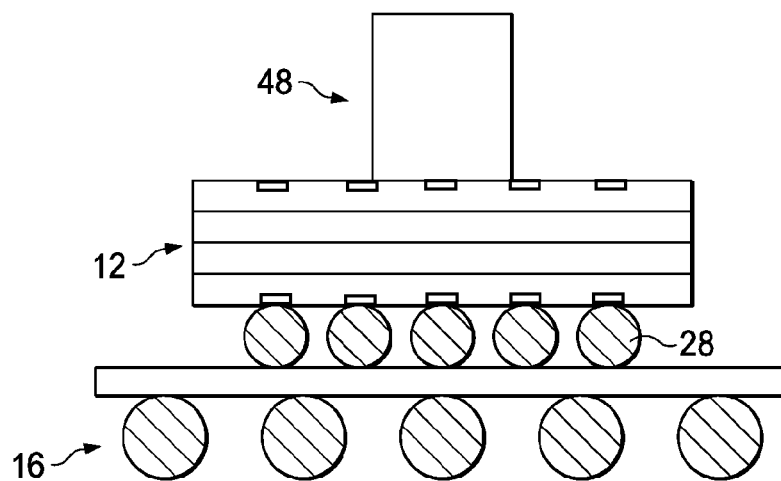


FIG. 3C

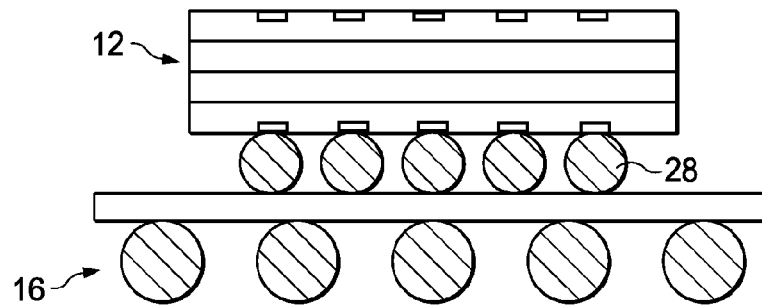


FIG. 3D

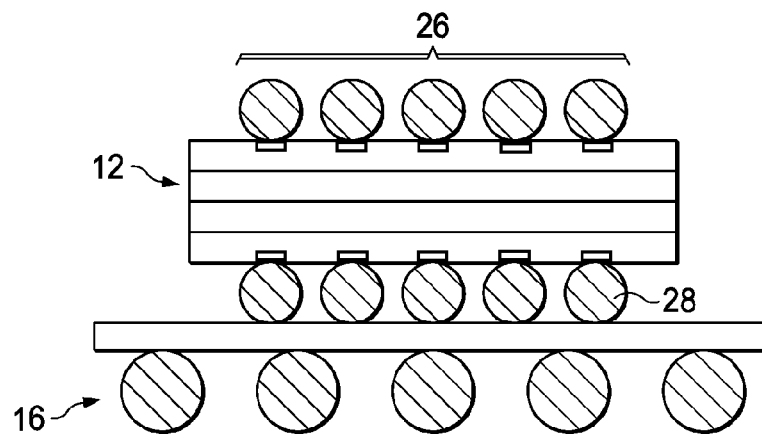


FIG. 3E

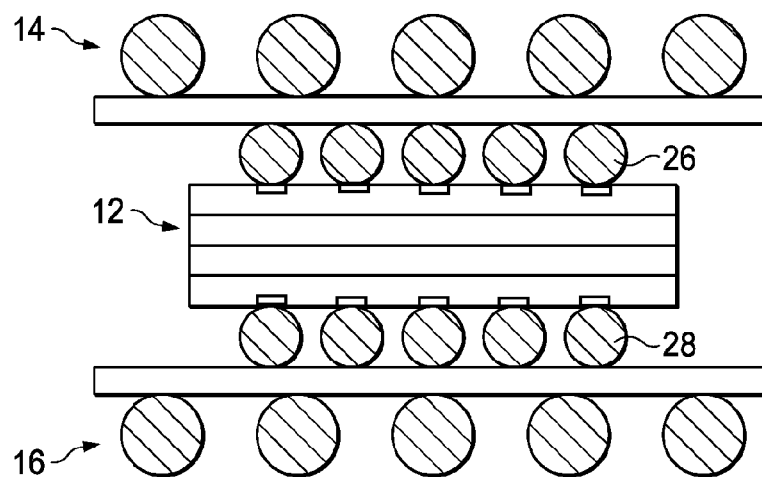


FIG. 3F

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## PACKAGE WITH MULTIPLE PLANE I/O STRUCTURE

### BACKGROUND

As the demand for smaller electronic products grows, manufacturers and others in the electronics industry continue to seek ways to reduce the size of the integrated circuits (ICs) used in the electronic products. In pursuit of that goal, three-dimensional (3D) type integrated circuit packaging techniques have been developed and used to produce three dimensional integrated circuits, or simply 3D ICs. Each 3D IC includes two or more chips stacked one on top of another and integrated both vertically and horizontally to generate a single circuit.

Because of the three dimensional structure of the 3D IC, the footprint of the stacked chips may be considerably smaller than the footprint of a conventional single layer chip. In other words, when viewed from above or below, the overall size of the stacked chips in the 3D IC may be smaller than the size of the conventional chip. However, due to the smaller footprint offered by the stacked chips in the 3D IC, it can be difficult for the 3D IC to contain all of the input/output (I/O) pads desired for a package.

Another way that the electronics industry is attempting to reduce the size of integrated circuits is by utilizing "flip chip" packaging. Flip chip microelectronic assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, another chip, wafer or carriers using conductive solder bumps on the chip bond pads.

In a typical flip chip assembly process, integrated circuits are created on a wafer. Thereafter, pads on a top surface of the integrated circuits are metallized. Next, conductive solder balls (i.e., dots or bumps) are deposited on the pads and the integrated circuits on the wafer are separated or cut from each other to form individual chips. Thereafter, each chip is "flipped" over and positioned so that the solder balls of the chip are aligned with mating connectors on the underlying external circuitry. Finally, the solder balls are re-melted and the mounted chip is under-filled using an electrically-insulating adhesive in order to complete the conventional flip-chip package.

In some cases, one of the 3D ICs described above is utilized in the fabrication of a flip chip package. To ensure that such a 3D IC package has a pitch suitable for larger, thicker printed circuit boards (PCBs), an interposer, substrate, or other suitable structure may be attached to one side of the 3D IC in order to fan out (a.k.a., bond out) the I/O pad of the 3D IC.

### BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates an embodiment three dimensional (3D) integrated circuit (IC) flip-chip style package;

FIG. 2A illustrates input/output (I/O) pads on a top surface of the package of FIG. 1;

FIG. 2B illustrates input/output (I/O) pads a bottom surface of the package of FIG. 1; and

FIGS. 3A-3F collectively schematically illustrate a method of forming the package of FIG. 1.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise

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indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

### DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.

The present disclosure will be described with respect to preferred embodiments in a specific context, namely a three dimensional (3D) integrated circuit (IC) flip-chip style package. The concepts in the disclosure may also apply, however, to other types of packages, semiconductor structures, or circuits.

Referring to FIG. 1, a three dimensional integrated circuit (3D IC) flip-chip style package 10 is illustrated. As will be more fully explained below, the package 10 provides numerous benefits and advantages. For example, the package 10 includes input/output connections on two different planes (e.g., the top and the bottom). In addition, even though the three dimensional integrated circuit within the package 10 offers only a small area for input/output connections, the two-sided configuration effectively doubles the number of input/output connections that can be formed on the three dimensional integrated circuit and utilized by the package.

As shown in FIG. 1, an embodiment package 10 generally includes a three dimensional integrated circuit 12, a first fan out structure 14, and a second fan out structure 16. In an embodiment, the three dimensional integrated circuit 12 includes a plurality of planar chips 18 (a.k.a., dies, integrated circuits, etc.) stacked upon each other. The chips 18 may have been singulated from a single wafer or a variety of different wafers prior to being stacked together.

The various chips 18 in the three dimensional integrated circuit 12 may include one or more of the following components: a logic device, a processor, a microprocessor, a memory (e.g., static random access memory (SRAM), etc.), an analog device, a digital device, an active device, a passive device, an antenna, a transmitter, a receiver, and so on. Notably, each chip 18 in the three dimensional integrated circuit 12 may utilize a single component, multiple similar components, or combinations of different components.

In an embodiment, the three dimensional integrated circuit 12 is both horizontally and vertically integrated. As such, the various components in one chip 18 may communicate with the other components of that same chip 18 as well as with the components of neighboring chips 18 in other layers of the three dimensional integrated circuit 12. To facilitate this communication between chips 18 of various layers, the three dimensional integrated circuit 12 may include vias, metallization, electrical connections, and so on.

While the stacked chips 18 of three dimensional integrated circuit 12 shown in FIG. 1 are generally vertically aligned, one or more of the chips 18 in the three dimensional integrated circuit 12 may be misaligned with a neighboring chip or chips 18 such that the three dimensional integrated circuit 12 includes an overhang. Likewise, while each of the chips 18 in the three dimensional integrated circuit 12 of FIG. 1 has the same size, the chips 18 of different layers may be of various sizes, with different widths, thicknesses, and so on. Moreover, while four of the chips 18 are depicted in FIG. 1, it

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should be recognized that more or fewer of the chips 18 may be included in the three dimensional integrated circuit 12 in practical applications.

As shown in FIG. 2A, which is a cross section of the three dimensional integrated circuit 12 alone taken generally along line 2A-2A, the three dimensional integrated circuit 12 has a top surface 20 defining a front plane. As shown, the top surface 20 includes several input/output (I/O) pads 22. As shown in FIG. 2B, which is a cross section of the three dimensional integrated circuit 12 alone taken generally along line 2B-2B, the three dimensional integrated circuit 12 has a bottom surface 24 defining a back plane or reverse plane. As shown, the bottom surface 24 also includes several input/output pads 22. In other words, the top chip 18 in the three dimensional integrated circuit 12 of FIG. 1 includes input/output pads 22 on the upper surface thereof and the bottom chip 18 in the three dimensional integrated circuit 12 of FIG. 1 includes input/output pads 22 on the bottom surface thereof.

In an embodiment, the three dimensional integrated circuit 12 has input/output pads 22 on at least two different planes, sides, surfaces, or faces. In an embodiment, the input/output pads 22 are disposed on opposing faces (e.g., top and bottom) of the three dimensional integrated circuit 12. In an embodiment, the input/output pads 22 are disposed on two different planes (e.g., top and left side, bottom and right side, etc.). In an embodiment, the input/output pads 22 are on parallel, spaced apart planes. In an embodiment, the input/output pads 22 are on perpendicular planes.

The input/output pads 22 in FIGS. 2A-2B are electrically coupled to the components and electrical structures included in the various chips 18 collectively forming the three dimensional integrated circuit 12. Therefore, the signals and functionality provided by the various chips 18 in the three dimensional integrated circuit 12 may be brought into, as well as sent out of, the three dimensional integrated circuit 12.

While the input/output pads 22 of FIGS. 2A-2B are square in shape, the input/output pads 22 may have a variety of other suitable shapes or configurations. By way of example, the input/output pads 22 may be in the shape of a circle, triangle, ellipse or oval, octagon, and so on. In addition, while the input/output pads 22 of FIGS. 2A-2B are equally-spaced around a periphery of the three dimensional integrated circuit 12, other arrangements are contemplated. Indeed, the input/output pads 22 may be positioned proximate the center of the three dimensional integrated circuit 12, at only the corners of the three dimensional integrated circuit 12, in an alternating pattern of pad and no pad around the periphery, at sides but not the center or the corners, or combinations or variations thereof.

While eight of the input/output pads 22 are depicted on each of the top surface 20 and the bottom surface 22 of the three dimensional integrated circuit 12, it should be recognized that more or fewer of the input/output pads 22 may be used in practical applications. In addition, while an equal number of the input/output pads 22 are depicted on both of the top surface 20 and the bottom surface 24 of the three dimensional integrated circuit 12, it should be recognized that the number of input/output pads 22 on the top surface 20 of the three dimensional integrated circuit 12 may disagree with the number of input/output pads 22 on the bottom surface 24 of the three dimensional integrated circuit 12. In an embodiment, the top surface 20 of the three dimensional integrated circuit 12 may have more of the input/output pads 22 than the bottom surface 24. In an embodiment, the bottom surface 24 of the three dimensional integrated circuit 12 may have more of the input/output pads 22 than the top surface 20.

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Referring back to FIG. 1, the input/output pads 22 on the top surface 20 of the three dimensional integrated circuit 12 are electrically coupled to corresponding pads on the first fan out structure 14 by electrical connectors 26. Likewise, the input/output pads on the bottom surface 24 of the three dimensional integrated circuit 12 are electrically coupled to corresponding pads on the second fan out structure 16 by electrical connectors 28. In an embodiment, the electrical connectors 26, 28 are solder bumps or other suitable electrical connectors. As shown in FIG. 1, the electrical connectors 26, 28 generally face toward the three dimensional integrated circuit 12 relative to the first and second fan out structures 14, 16.

Still referring to FIG. 1, in an embodiment the first fan out structure 14 includes a substrate 30 and electrical connectors 32. In an embodiment, the substrate 30 is a build-up substrate, a laminate substrate, or some other suitable substrate. In an embodiment, the substrate 30 is an interposer. In an embodiment, the substrate 30 is free or substantially free of active components. In an embodiment, the substrate 30 is a dielectric or other insulating material incorporating sufficient metallization to electrically couple the electrical connectors 26 to the electrical connectors 32.

In an embodiment, the electrical connectors 32 of the first fan out structure 14 comprise a ball grid array (BGA). As shown in FIG. 1, the electrical connectors 32 of the first fan out structure 14 generally face away from the three dimensional integrated circuit 12.

Still referring to FIG. 1, in an embodiment the second fan out structure 16 includes a substrate 34 and electrical connectors 36. In an embodiment, the substrate 34 is a build-up substrate, a laminate substrate, or some other suitable substrate. In an embodiment, the substrate 34 is an interposer. In an embodiment, the substrate 34 is free or substantially free of active components. In an embodiment, the substrate 34 is a dielectric or other insulating material incorporating sufficient metallization to electrically couple the electrical connectors 28 to the electrical connectors 36. In an embodiment, the substrate 34 of the second fan out structure 16 is different than the substrate 30 of the first fan out structure 14.

In an embodiment, the electrical connectors 36 of the second fan out structure 16 comprise a ball grid array (BGA). As shown in FIG. 1, the electrical connectors 36 of the second fan out structure 16 generally face away from the three dimensional integrated circuit 12. In an embodiment, the electrical connectors 36 of the second fan out structure 16 are different than the electrical connectors 32 of the first fan out structure 14.

In an embodiment, a pitch 38 of the electrical connectors 32 from the first fan out structure 14 and a pitch 40 of the electrical connectors 36 from the second fan out structure 16 are each larger or greater than a pitch 42 of the electrical connectors 26 coupled to the top surface 20 of the three dimensional integrated circuit 12 and a pitch 44 of the electrical connectors 28 coupled to the bottom surface 24 of the three dimensional integrated circuit 12.

In an embodiment, the pitch 38 of the electrical connectors 32 from the first fan out structure 14 is different from the pitch 40 of the electrical connectors 36 from the second fan out structure 16. In an embodiment, the pitch 42 of the electrical connectors 26 coupled to the top surface 20 of the three dimensional integrated circuit 12 is different from the pitch 44 of the electrical connectors 28 coupled to the bottom surface 24 of the three dimensional integrated circuit 12.

In an embodiment, the first and second fan out structures 14, 16 may be replaced with fan in or other suitable structures to provide the package 10 with other desirable characteristics

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and properties. In other words, in an embodiment the pitch **38**, **40** of the electrical connectors **38**, **40** on the fan out structures **14**, **16** may be the same as, or substantially the same as, the pitch **42**, **44** of the electrical connectors **26**, **28**.

Still referring to FIG. 1, a molding compound **46**, encapsulant, or other suitable material may be used to protect or encapsulate the three dimensional integrated circuit **12**. As shown, the molding compound **46** is generally disposed between the first and second fan out structures **14**, **16**. In an embodiment, the molding compound **46** extends laterally beyond a periphery of the first and second fan out structures **14**, **16**. In an embodiment, horizontal surfaces of the molding compound **46** are co-planar with exterior surfaces of the first and second fan out structures **14**, **16**. Although not shown, an underfill material may be used to protect or encapsulate the electrical connectors **26**, **28** disposed between the first and second fan out structures **14**, **16** and the three dimensional integrated circuit **12**.

Referring collectively to FIGS. 3A-3F, a method of forming the package **10** of FIG. 1 is schematically illustrated. As shown in FIG. 3A, the three dimensional integrated circuit **12** is temporarily grasped or seized using a circuit holding device **48** (a.k.a., carrier, grabber, etc.). As shown in FIG. 2A, space between the input/output pads **22** on the top surface **20** was reserved to provide a temporary attachment location for the circuit holding device **48**. Indeed, in the embodiment of FIG. 2A, the reserved space comprises the center portion of the top chip **18**, which is not occupied by input/output pads **22**. In an embodiment, the spaced reserved for the circuit holding device **48** may be different depending on the configuration of the input/output pads **22**.

While the circuit holding device **48** of FIG. 3A is depicted as holding or supporting the three dimensional integrated circuit **12** from below, in an embodiment the circuit holding device **48** may suitably hold or secure the three dimensional integrated circuit **12** from above. In such an embodiment, the reserved space comprises the center portion of the bottom chip **18**, which is not occupied by input/output pads **22**.

After the three dimensional integrated circuit **12** is secured in place by the circuit holding device **48** as shown in FIG. 3A, the electrical connectors **28** (e.g., solder bumps) are formed on the input/output pads **22** on the reverse side plane of the three dimensional integrated circuit **12** as shown in FIG. 3B. Thereafter, as shown in FIG. 3C, the three dimensional integrated circuit **12** is flipped using the circuit holding device **48**.

Once flipped, the three dimensional integrated circuit **12** is mounted to the second fan out structure **16**. In an embodiment, the three dimensional integrated circuit **12** is mounted to the second fan out structure **16** by reflowing solder bumps used for the electrical connectors **28**. In an embodiment, the second fan out structure **16** comprises a BGA substrate, as described above. As depicted in FIG. 3C, when the three dimensional integrated circuit **12** is mounted to the second fan out structure **16**, the front side plane faces upward.

Next, as shown in FIG. 3D, the circuit holding device **48** is removed. With the circuit holding device **48** disengaged from the three dimensional integrated circuit **12**, the electrical connectors **26** (e.g., solder bumps) are formed on the input/output pads **22** on the front side plane of the three dimensional integrated circuit **12** as shown in FIG. 3E. Thereafter, as shown in FIG. 3F, the first fan out structure **14** is mounted to the three dimensional integrated circuit **12**. In an embodiment, the three dimensional integrated circuit **12** is mounted to the first fan out structure **14** by reflowing solder bumps used for the electrical connectors **26**. In an embodiment, the first fan out structure **14** comprises a BGA substrate, as described above.

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Finally, as shown in FIG. 1, the molding compound **46** may be introduced between the first and second fan out structures **14**, **16** and around the three dimensional integrated circuit **12** to complete the package **10**. It should be recognized that other or additional processing steps may be performed to complete or augment the package **10** of FIG. 1 in practical applications. Also, some of the process steps mentioned herein may be optionally omitted from the method. For example, the flipping step may be removed from the fabrication process if a packaging technique other than flip chip style packaging is performed.

From the foregoing, it should be recognized that the embodiment package **10** of FIG. 1 provides numerous advantages and benefits. Indeed, the package **10** includes two-sided bonding. In addition, the package **10** doubles the number of input/outputs available from the three dimensional integrated circuit **12**. In addition, the manufacture or fabrication of the package **10** is relatively easy to fabricate. Moreover, the benefits and methodology disclosed herein for the flip chip style package **10** are equally suitable for other similar types of packages.

An embodiment package includes a three dimensional integrated circuit with first input/output pads on a first side and second input/output pads on a second side, a first fan out structure electrically coupled to the first input/output pads on the first side of the three dimensional integrated circuit, and a second fan out structure electrically coupled to the second input/output pads on the second side of the three dimensional integrated circuit.

An embodiment package includes a three dimensional integrated circuit with first input/output pads on a first side and second input/output pads on a second side, a first substrate having first electrical connectors on opposing sides, the first electrical connectors extending toward the three dimensional integrated circuit electrically coupled with the first input/output pads, and a second substrate having second electrical connectors on opposing sides, the second electrical connectors extending toward the three dimensional integrated circuit electrically coupled with the second input/output pads.

An embodiment method of forming a package includes mounting a three dimensional integrated circuit to one side of a first fan out structure, and mounting a second fan out structure on an opposing side of the three dimensional integrated circuit.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A package, comprising:

- a three dimensional integrated circuit with first input/output pads on a first side and second input/output pads on a second side, wherein the first input/output pads have a first pitch different from a second pitch of the second input/output pads;
- a first fan out structure electrically coupled to the first input/output pads on the first side of the three dimensional integrated circuit; and
- a second fan out structure electrically coupled to the second input/output pads on the second side of the three dimensional integrated circuit.



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2. The package of claim 1, wherein the first side and the second side are on opposite sides of the three dimensional integrated circuit.

3. The package of claim 1, wherein the first fan out structure comprises a first ball grid array (BGA) electrically coupled to a first substrate.

4. The package of claim 3, wherein the second fan out structure comprises a second ball grid array (BGA) electrically coupled to a second substrate.

5. The package of claim 4, wherein at least one of the first substrate and the second substrate is a build-up substrate or a laminate substrate.

6. The package of claim 4, wherein at least one of the first substrate and the second substrate is an interposer.

7. The package of claim 1, wherein the first fan out structure is electrically coupled to the first input/output pads by first solder bumps and the second fan out structure is electrically coupled to the second input/output pads by second solder bumps.

8. The package of claim 7, wherein the first fan out structure comprises a first ball grid array (BGA) with a third pitch, the second fan out structure comprises a second ball grid array (BGA) with a fourth pitch, the first and second pitch each less than the third pitch and the fourth pitch.

9. The package of claim 1, wherein the first fan out structure includes a first ball grid array (BGA) with a third pitch and the second fan out structure includes a second ball grid array (BGA) with a fourth pitch different from the third pitch.

10. A package, comprising:

a three dimensional integrated circuit, the three dimensional integrated circuit comprising a first integrated circuit die on a first side and a second integrated circuit die on a second side, the first integrated circuit die having first input/output pads on the first side, the second integrated circuit die having second input/output pads on the second side, the first side being an opposite side of the three dimensional integrated circuit from the second side;

a first substrate having first electrical connectors on opposing sides, a first subset of the first electrical connectors extending toward the three dimensional integrated circuit and electrically coupled with the first input/output pads; and

a second substrate having second electrical connectors on opposing sides, a first subset of the second electrical connectors extending toward the three dimensional integrated circuit and electrically coupled with the second input/output pads, wherein the three dimensional integrated circuit is interposed between the first substrate and the second substrate.

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11. The package of claim 10, wherein the first subset of the first electrical connectors and the first subset of second electrical connectors comprise solder bumps.

12. The package of claim 10, wherein each of a second subset of the first electrical connectors facing away from the three dimensional integrated circuit and a second subset of the second electrical connectors facing away from the three dimensional integrated circuit comprise a ball grid array (BGA).

13. The package of claim 10, wherein a second subset of the first electrical connectors facing away from the three dimensional integrated circuit have a larger pitch than the first subset of the first electrical connectors, and a second subset of the second electrical connectors facing away from the three dimensional integrated circuit have a larger pitch than the first subset of the second electrical connectors.

14. The package of claim 10, wherein the first substrate and the second substrate are each free of active electrical devices.

15. A method of forming a package, comprising:

mounting a three dimensional integrated circuit to a first side of a first fan out structure, the first fan out structure having first external connectors on a second side of the first fan out structure, the first side and the second side being opposite sides of the first fan out structure; and mounting a second fan out structure on an opposing side of the three dimensional integrated circuit from the first fan out structure, the second fan out structure having second external connectors on a side of the second fan out structure opposite from the three dimensional integrated circuit.

16. The method of claim 15, further comprising flipping the three dimensional integrated circuit prior to the mounting the second fan out structure.

17. The method of claim 15, further comprising encapsulating the three dimensional integrated circuit with molding compound, the molding compound disposed between the first and second fan out structures.

18. The method of claim 17, wherein the molding compound extends along sidewalls of a first integrated circuit die of the three dimensional integrated circuit.

19. The method of claim 15, further comprising reflowing first solder bumps to mount the first fan out structure to first input/output pads on the one side of the three dimensional integrated circuit and reflowing second solder bumps to mount the second fan out structure to second input/output pads on the opposing side of the three dimensional integrated circuit.

20. The method of claim 15, further comprising mounting the first fan out structure and the second fan out structure to the three dimensional integrated circuit such that a ball grid array (BGA) of each faces in opposite directions.

\* \* \* \* \*